WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a first layer having a plurality of signal wires; and

a second layer adjacent to the first layer having a plurality of signal wires, wherein the signal wires in the first and second layers are substantially parallel with each other.

2. The semiconductor device of claim 1, wherein adjacent signal wires are located in an alternating pattern in the first and second layers.

3. The semiconductor device of claim 2, wherein the alternating pattern has every other signal wire residing in the same layer.

4. The semiconductor device of claim 1, wherein power supply and ground wires are located in both the first layer and the second layer.

5. The semiconductor device of claim 4, wherein power supply and ground wires are located in the same respective position in each layer.

6. The semiconductor device of claim 1, further comprising:

at least one additional layer adjacent to the first and second layer, wherein signal wires in the at least one additional layer are substantially parallel to signal wires in the first and second layers

7. The semiconductor device of claim 6, wherein adjacent signal wires are located in an alternating pattern in the first, second, and at least one additional layer.

8. The semiconductor device of claim 1, further comprising:

N layers, wherein N is greater than two and wherein the first and second layers are any two adjacent layers in the N layers.

9. The semiconductor device of claim 1, wherein the semiconductor device is a microprocessor.

10. The semiconductor device of claim 1, wherein the first layer and second layer have similar process parameters.

11. The semiconductor device of claim 2, wherein the pluralities of signal wires in the first and second layer are a first set of signal wires configured to carry a first set of related signals.

12. The semiconductor device of claim 11, further comprising:

a second set of signal wires that are replicated in the first and second layers.

13. The semiconductor device of claim 1, further comprising:

additional signal wires in the second layer that are located substantially orthogonal to the plurality of signal wires in the first layer.

14. The semiconductor device of claim 1, wherein the plurality of signal wires in the first layer is a set of related signal wires and wherein the plurality of signal wires in the second layer is a replication of the plurality of signal wires in the first layer.

15. A method of adding metal layers in a semiconductor device, the method comprising:

adding a second layer to a first layer, wherein the second layer is adjacent to the first layer; and

distributing a plurality of signal wires between the first layer and the second layer, wherein the plurality of signal wires are substantially parallel with each other.

16. The method of claim 15, further comprising:

distributing adjacent signal wires in an alternating pattern in the first and second layers.

17. The method of claim 15, further comprising:

identifying a critical signal wire from the plurality of signal wires in the first layer; and

assigning signal wires adjacent to the critical signal wire to the second layer.

18. The method of claim 17, wherein identifying the critical signal wire comprises:

analyzing an existing microprocessor design to identify frequency limiting signal wires; and

identifying one of the frequency limiting signal wires as the critical signal wire.

19. The method of claim 15, further comprising:

inserting at least one of a power supply wire and a ground wire in the second layer.

20. The method of claim 19, wherein power supply and ground wires are located in the same respective position in each layer.

21. The method of claim 15, further comprising:

providing at least one additional layer adjacent to first and second layers, wherein signal wires in the at least one additional layer are substantially parallel to signal wires in the first and second layers.

22. The method of claim 21, further comprising:

distributing signal wires in an alternating pattern in the first layer, the second layer and the at least one additional layer.

23. The method of claim 15, further comprising:

forming the first layer and second layer using the same process.

24. The method of claim 15, wherein the semiconductor device has N layers, wherein N is greater than two and wherein the first and second layers are any two adjacent layers in the N layers.

25. The method of claim 15, wherein the semiconductor device is a microprocessor.

26. The method of claim 15, wherein the plurality of signal wires in the first and second layers are a first set of signal wires configured to carry related signals.

27. The method of claim 15, wherein distributing the plurality of signal wires comprises:

replicating a set of signal wires in both the first and second layers.

28. The method of claim 15, further comprising:

arranging additional signal wires in the second layer substantially orthogonal to the signal wires in the first layer.

29. A system comprising:

a microprocessor; and

an off-die component in communication with the microprocessor; wherein the microprocessor comprises:

a first layer having a plurality of signal wires; and

a second layer adjacent to the first layer having a plurality of signal wires, wherein the signal wires in the first and second layers are substantially parallel with each other.

30. The microprocessor of claim 29, further comprising:

at least one additional layer adjacent to the first and second layers, wherein signal wires in the at least one additional layer are substantially parallel to signal wires in the first and second layers.